

BIDHAN BISWAS

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EDUCATION

Rajiv Gandhi Institute of Petroleum Technology

B.Tech - Electronic Engineering

2022 – 2026

Amethi, Uttar Pradesh

Govt. Rajendra College

Class-12th ; PERCENTAGE - 80

Faridpur, Bangladesh

Faridpur Zilla School

Class-10th ; PERCENTAGE- 90

Faridpur, Bangladesh

COURSEWORK / SKILLS

- Digital Circuit Design
- Analog Circuit Design
- Signals and Systems
- Hardware Described language (HDL)
- Embedded System
- Network Analysis And Synthesis
- Solid State Electronics Devices
- Control System

PROJECTS

A Fully Synthesizable All-Digital Phase-Locked Loop with Portable Architecture [↗](#) | ongoing

- Using the Verilog Hardware Description Language, a novel and portable enough circuitry arrangement is designed by using the ADPLL- All-Digital Phase-Locked Loop.
- It could preferably contain DCO- Digitally Controllable Oscillator that could be varied as needed

ADC and SENSOR interfacing with FPGA using SPI Protocol [↗](#) |

ongoing

- The project focuses on how SPI protocol transfer data and information between sensor and ADC with FPGA.

A VLSI On-Chip Analog High-Order Low-Pass Filter Performance Evaluation Strategy [↗](#) | ongoing

- This paper presents a strategy for evaluation of an analog high-order low-pass filter.
- In the proposed strategy, the evaluation procedure is divided into three modes, first, to estimate the passband characteristic, second, to estimate the stopband characteristic, and finally, to evaluate the performance of the analog filter by the analysis of the relationship between the attenuations at the passband and stopband.

TECHNICAL SKILLS

Languages: C, Embedded-C , Matlab .

Hardware Described Languages: Verilog , System Verilog, VHDL

EDA Tools: Xilinx Vivado, Xilinx IDE, Arduino IDE

ACHEIVEMENTS

- Study In India(SII) Scholar
- Solved 100+ Problems across **HDL Bits** and Simulated design using **EDA playground**

POSITION OF RESPONSIBILITY

- Coordinator , Tinkering Lab (Science and Technical Council RGIPT).